sius for a period between about 1 second and about 4 hours. To inhibit decomposition, a capping layer may be deposited on the indium-containing film prior to the thermal or annealing treatment. The capping layer may comprise at least one of GaN, AN, AlGaN, SiO_2, and SiN_x. At least an outermost portion of the indium-containing film has a wurtzite structure, is substantially relaxed and unstrained, and is well-crystallized. The x-ray diffraction full-width-at-half-maximum (FWHM) of the lowest-order on-axis (symmetric) reflection may be less than about 500 arc-sec, less than about 300 arc-sec, less than about 200 arc-sec, less than about 150 arc-sec, or less than about 100 arc-sec. The x-ray diffraction full-width-at-half-maximum of the lowest-order off-axis (asymmetric) reflection may be less than about 1000 arc-sec, less than about 800 arc-sec, less than about 500 arc-sec, less than about 300 arc-sec, less than about 200 arc-sec, less than about 150 arc-sec, or less than about 100 arc-sec. In a specific embodiment, the indium-containing film has a c-plane orientation, an x-ray rocking-curve (002) reflection FWHM less than about 300 arc-sec and a (102) reflection FWHM less than about 1000 arc-sec. In another specific embodiment, the indium-containing film has a c-plane orientation, an x-ray rocking-curve (002) reflection FWHM less than about 150 arc-sec and a (102) reflection FWHM less than about 300 arc-sec.

In some embodiments, an additional indium-containing nitride layer is deposited. The second deposition may be performed in a second reactor, after cooldown from the second temperature and removal from the first reactor. In some embodiments, the second deposition is performed using MOCVD. In other embodiments, the second deposition is performed using hydride vapor phase epitaxy (HVPE). The additional indium-containing nitride layer may have a thickness between about 1 micron and about 100 millimeters, or between about 20 microns and about 10 millimeters, or between about 100 microns and about 5 millimeters. The additional deposition thickness can assist in reducing threading dislocation density, and thus improve crystallinity of the indium-containing nitride layer.

In some embodiments, the indium-containing nitride layer is removed from the substrate. The substrate may be removed by spontaneous delamination, by laser liftoff, by selective chemical etching, or the like, according to methods that are known in the art, to produce a free-standing indium-containing nitride boule or wafer. It is to be appreciated that the indium-containing nitride layer provided by the methods described in this invention is substantially near its native, strain-free state. For example, the in-plane lattice constant for a (0001) indium-gallium-nitride of the present invention will be higher than that of GaN (3.19 Å). In particular, the in-plane lattice constant of the (0001) indium-gallium-nitride layer may be greater than 3.20 Å, greater than 3.22 Å, greater than 3.24 Å, greater than 3.26 Å, or greater than 3.28 Å. The relationship between materials parameters and compositions for semiconductor alloys are described, for example, in I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan, J. Appl. Phys. 89, 11, pp. 5815-5875 (2001), which is hereby incorporated by reference in its entirety. Therefore, the teachings in this invention provide a large-area, homogeneous, near-strain-free indium-containing nitride layer which overcomes the limitations of the prior art and can be employed for improved optoelectronic devices.

One or more active layers may be deposited on the well-crystallized indium-containing nitride layer. The active layer may be incorporated into an optoelectronic or electronic devices such as at least one of a light emitting diode, a laser diode, a photodetector, an avalanche photodiode, a transistor, a rectifier, and a thyristor; one of a transistor, a rectifier, a Schottky rectifier, a thyristor, a p-i-n diode, a metal-semiconductor-metal diode, high-electron mobility transistor, a metal semiconductor field effect transistor, a metal oxide field effect transistor, a power metal oxide semiconductor field effect transistor, a power metal insulator semiconductor field effect transistor, a bipolar junction transistor, a metal insulator field effect transistor, a heterojunction bipolar transistor, a power insulated gate bipolar transistor, a power vertical junction field effect transistor, a cascode switch, an inner sub-band emitter, a quantum well infrared photodetector, a quantum dot infrared photodetector, a solar cell, and a diode for photoelectrochemical water splitting and hydrogen generation.

While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present disclosure which is defined by the appended claims.

What is claimed is:

1. A method for fabricating a gallium, indium, and nitrogen containing material, the method comprising:

providing a substrate having a surface region;

forming a first thickness of material having a first indium-rich concentration;

forming a second thickness of material having a first indium-poor concentration overlying the first thickness of material;

forming a third thickness of material having a second indium-rich concentration overlying the second thickness of material to form a sandwiched structure comprising at least the first thickness of material, the second thickness of material, and third thickness of material; and

processing the sandwiched structure using at least a thermal process to cause formation of well-crystallized, relaxed material within a vicinity of a surface region of the sandwiched structure; and

wherein the sandwiched structure has an overall thickness of 100 nm or greater.

2. A method for fabricating a gallium, indium, and nitrogen containing material, the method comprising:

providing a substrate having a surface region;

forming a first thickness of material having a first indium-rich concentration;

forming a second thickness of material having a first indium-poor concentration overlying the first thickness of material;

forming a third thickness of material having a second indium-rich concentration to form a sandwiched structure comprising at least the first thickness of material, the second thickness of material, and third thickness of material; and

processing the sandwiched structure using at least a thermal process to cause formation of well-crystallized, relaxed material within a vicinity of a surface region of the sandwiched structure wherein

the well-crystallized, relaxed material has a full-width-at-half-maximum of the lowest-order symmetric x-ray reflection of 300 arc-seconds or less; and

the sandwiched structure has an overall thickness of 100 nm or greater.

3. The method of claim **2** wherein the substrate is selected from a material consisting of gallium nitride, aluminum nitride, sapphire, silicon carbide, $MgAl_2O_4$ spinel, ZnO, BP, $ScAlMgO_4$, $YFeZnO_4$, MgO, Fe_2NiO_4, $LiGa_5O_8$, Na_2MoO_4,